

ABSTRACT

A PWM buffer circuit includes a duty cycle converting circuit and a frequency-fixed PWM signal generating circuit. The duty cycle converting circuit is used for receiving a first PWM signal and then generating a duty cycle reference voltage on the basis of the first PWM
5 signal. The duty cycle reference voltage is a one-to-one mapping function of the first duty cycle. The frequency-fixed PWM signal generating circuit is used for receiving the duty cycle reference voltage and then outputting a second PWM signal with a fixed frequency. The second PWM signal has a second duty cycle, which is determined in accordance with the duty cycle reference voltage. In addition, the second duty cycle is a one-to-one mapping
10 function of the duty cycle reference voltage.